Remarks/Arguments

Summary

By this Amendment, claims 1 and 7 have been revised, and accordingly, claims 1-12 remain pending in the application.

Previous Submitted IDS

On March 31, 2003, Applicants filed an Information Disclosure Statement (IDS), a Form PTO-1449, and a copy of the reference (US 6117778 – Jones et al.) list in the Form PTO-1449. Copies of the IDS and Form PTO-1449, and a returned postcard receipt, are attached.

Acknowledgement on the record of the IDS and consideration of the cited reference are respectfully requested.

Amendments

Independent claims 1 and 7 have been revised to clarify that the present invention is directed to removing the material layer coated on the sidewall of the wafer. Support for these revisions can be found in the drawings, and at least at page 10, lines 15 and 20, and page 12, line 9, of the original specification.

Also, the specification has been revised to improve the clarity of the disclosure, and as in claims 1 and 7, to clarify that the present invention is directed to removing the material layer coated on the sidewall of the wafer. While some new language may appear in the amendments to the specification, Applicants contend that any such new language is at least inherently disclosed by the original specification and drawings, and accordingly, Applicants further contend that no new matter has been added.

35 U.S.C. ¶102 and ¶103

Claims 1 and 3-6 were rejected under 35 U.S.C. ¶102 or ¶103 as being unpatentable over Lo et al. (US 5783097), taken alone or in combination with Liu et al. (US 6287961), for the reasons stated at pages 2-4 of the Office Action. Claims 1-2 and 7-12 were rejected under 35 U.S.C. ¶103 as being unpatentable over Weng et al. (US 5879577), in view of the admitted prior art or Liu et al., for the reasons stated at pages 4-6 of the Office Action. However, Applicants respectfully contend that the now-pending claims 1-12 define over the cited references, and in view of the following representations, reconsideration of the rejections under 35 U.S.C. ¶102 and ¶103 is requested.

As recited in the now-pending claims, the present invention is directed to removing the material layer coated on the sidewall of the wafer. The sidewall is considered a dead zone region since the material layer thereon cannot be planarized by the CMP process, or before or after the CMP process. Any material present on the sidewall of wafer functions as a potential source of particle contamination, and the present invention is directed to removing that potential source of particle contamination.

The references cited by the Examiner do not teach removal of material from the sidewall of the wafer as in the presently claimed invention. That is, Lo et al. is directed to avoiding damage to dielectric material present at the flat surface edge of an integrated circuit wafer. Likewise, Weng et al. is directed to the selective etching of material along the peripheral surface of a circular substrate, and more particularly, to the etching of a so-called edge bead from an SOG layer.

The presently claimed invention is therefore distinguished from the cited references at least by the etching of a material layer coated on the sidewall of the wafer, thereby preventing particle contamination otherwise caused by such a material layer.

For at least the reasons stated above, Applicants respectfully contend that claims 1-12 are neither anticipated by, nor rendered obvious in view of, the teachings of the cited references, taken individually or in combination.

Conclusion

No other issues remaining, reconsideration and favorable action upon the claims 1-12 now present in the application are requested.

Respectfully submitted,

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July 30, 2003

Attachments: Copies of IDS, Form PTO-1449, and returned postcard receipt, all dated March 31, 2003

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ABSTRACT OF THE DISCLOSURE

A method of fabricating a semiconductor device to prevent contaminating particle formation. The method includes depositing a layer having a selected thickness on a wafer and then planarizing the deposited layer. A photoresist layer is then coated on the deposited layer. ~~An edge~~ A portion of the coated photoresist layer is removed to thereby expose a dead zone region of the deposited layer, with the dead zone region corresponding to a portion of the initial deposited layer which is not removed during the planarization process. The exposed deposited layer of the dead zone region is then etched, and the photoresist layer remaining on the wafer is stripped to form the desired pattern.